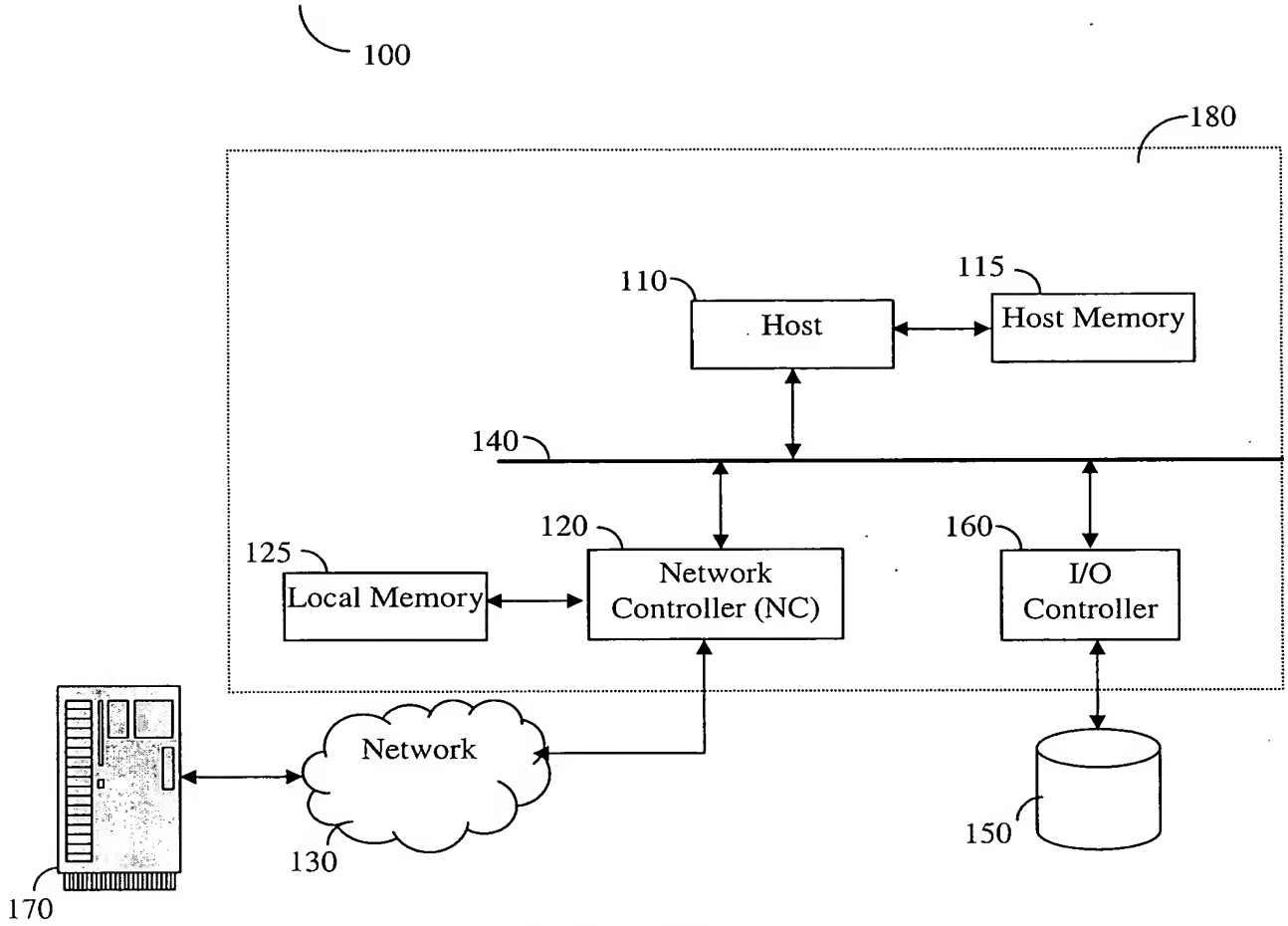


FIGURE 1(PRIOR ART)

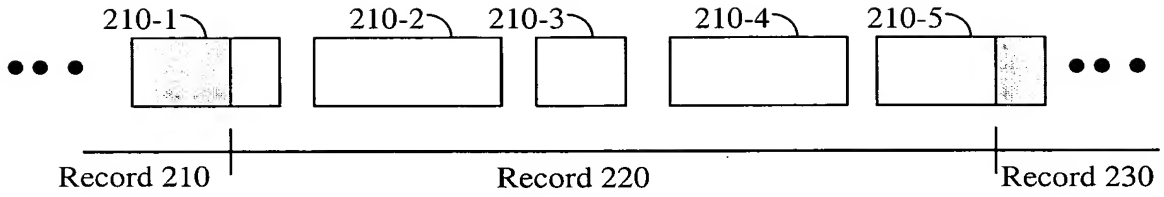


FIGURE 2 (PRIOR ART)

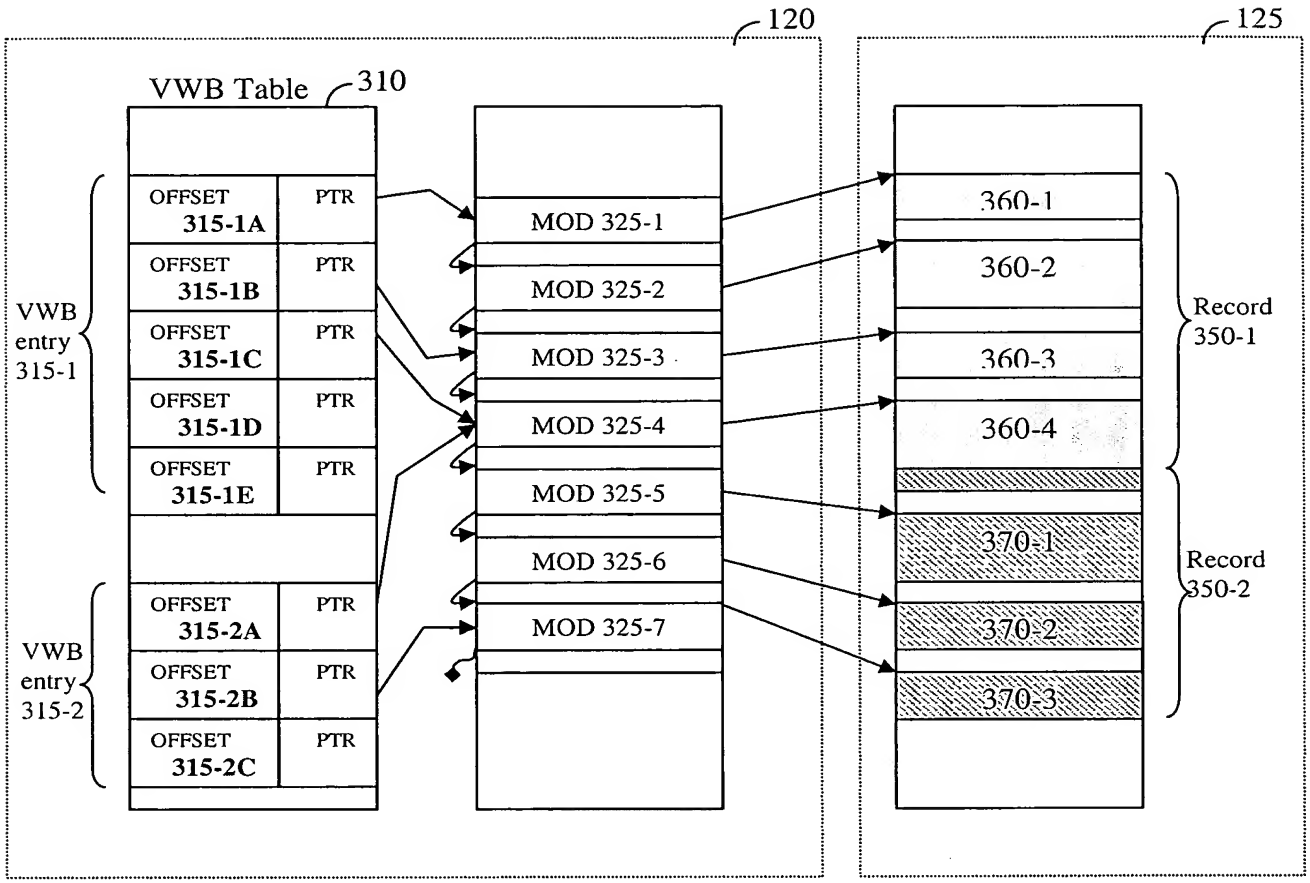
120
125
VWB Table
310
OFFSET
315-1A
PTR
OFFSET
315-1B
PTR
OFFSET
315-1C
PTR
OFFSET
315-1D
PTR
OFFSET
315-1E
PTR
VWB
entry
315-1
OFFSET
315-2A
PTR
OFFSET
315-2B
PTR
OFFSET
315-2C
PTR
VWB
entry
315-2
MOD 325-1
MOD 325-2
MOD 325-3
MOD 325-4
MOD 325-5
MOD 325-6
MOD 325-7
360-1
360-2
360-3
360-4
370-1
370-2
370-3
Record
350-1
Record
350-2

FIGURE 3

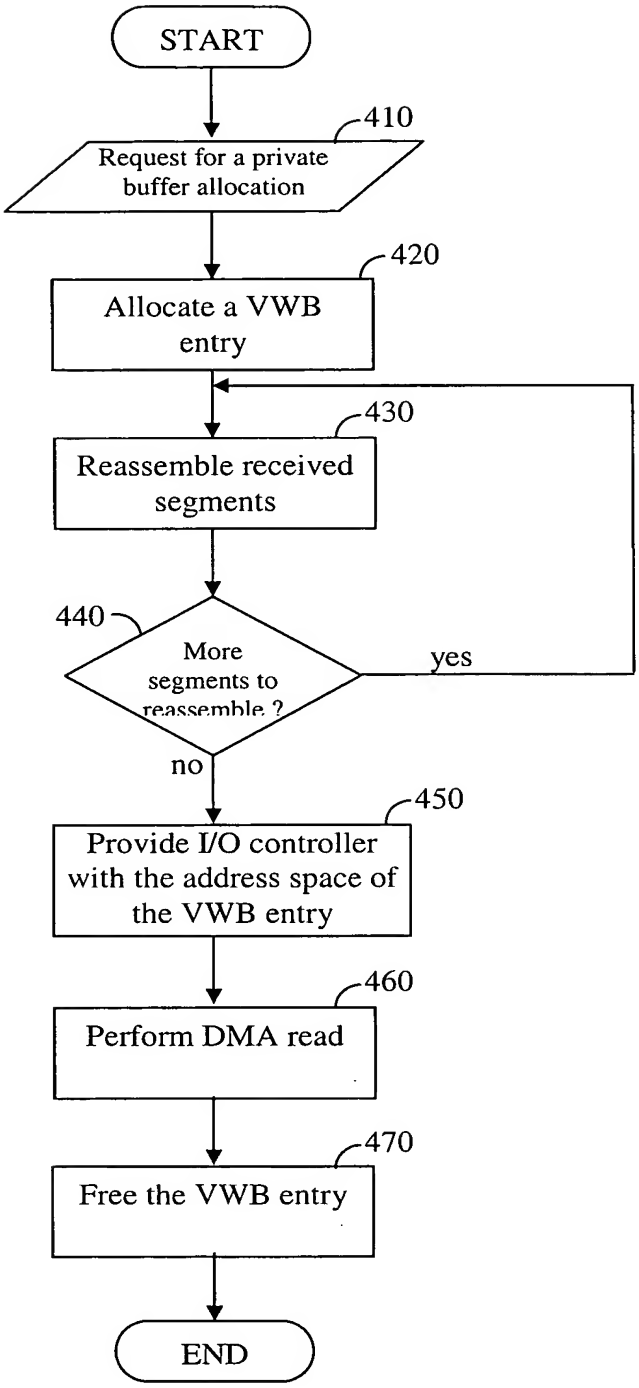
START
410
Request for a private buffer allocation
420
Allocate a VWB entry
430
Reassemble received segments
440
More segments to reassemble ?
yes
no
450
Provide I/O controller with the address space of the VWB entry
460
Perform DMA read
470
Free the VWB entry
END

FIGURE 4

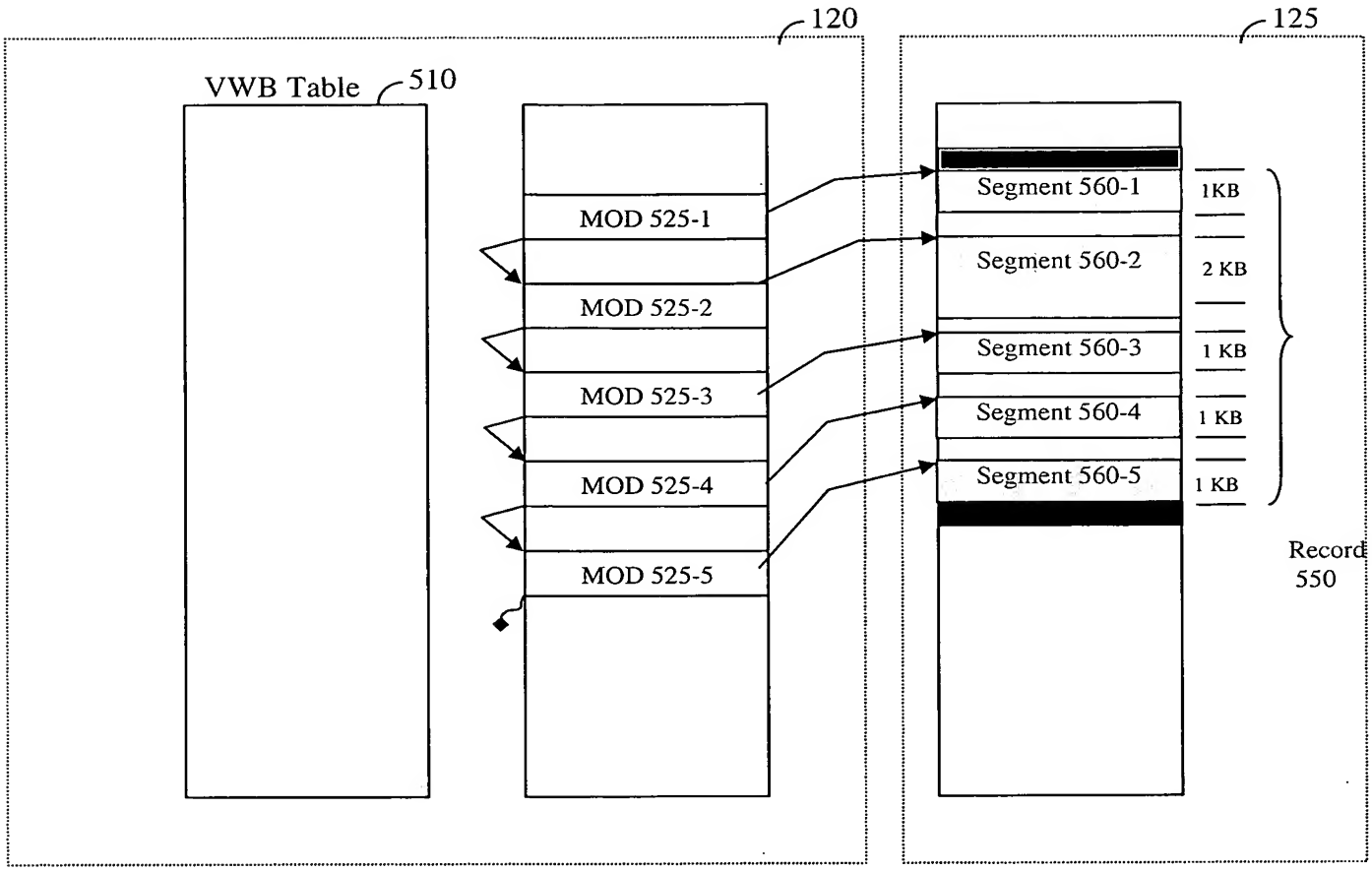
120
125
VWB Table
510
MOD 525-1
MOD 525-2
MOD 525-3
MOD 525-4
MOD 525-5
Segment 560-1
Segment 560-2
Segment 560-3
Segment 560-4
Segment 560-5
1KB
2 KB
1 KB
1 KB
1 KB
Record
550

FIGURE 5A

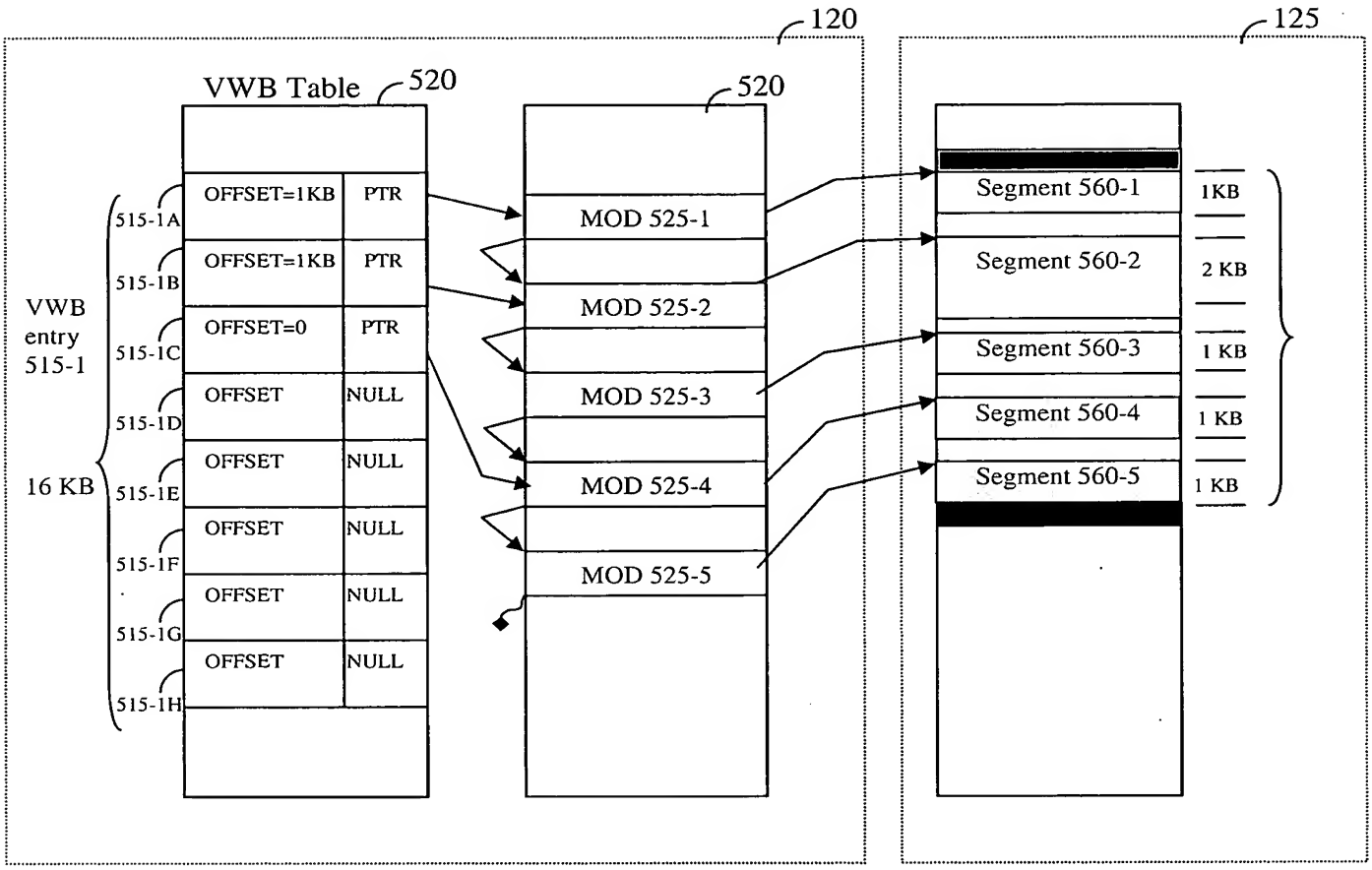
120
125
VWB Table
520
520
OFFSET=1KB
PTR
OFFSET=1KB
PTR
OFFSET=0
PTR
OFFSET
NULL
OFFSET
NULL
OFFSET
NULL
OFFSET
NULL
OFFSET
NULL
515-1A
515-1B
515-1C
515-1D
515-1E
515-1F
515-1G
515-1H
VWB entry 515-1
16 KB
MOD 525-1
MOD 525-2
MOD 525-3
MOD 525-4
MOD 525-5
Segment 560-1
Segment 560-2
Segment 560-3
Segment 560-4
Segment 560-5
1KB
2 KB
1 KB
1 KB
1 KB

FIGURE 5B